Mobile DRAM Standard Formulation

Chun-Lung Hsu, Jenn-Shyang Chiou and Wen-Hsin Peng

Abstract — **Mobile DRAM is widely employed in portable electronic devices due to its feature of low-power consumption. Recently, as the market trend renders integration of various features in one chip, mobile DRAM is required to have not only low-power consumption but also high capacity and high speed requirement. Due to the mobile devices of smartphone and tablet are more popular in ordinary lives and dominate people's living behavior, the demand of mobile DRAMs is steadily on the increase in the electronics market. This paper intends to expose the standard formulating information of mobile DRAMs such as, low-power double data rate (LPDDR) series memories and Wide-I/O (WIO) DRAMs from the international organization of JEDEC.**

Index Terms — **Mobile DRAM; low-power; LPDDR; WIO**

I. Introduction

The mobile era has emerged with a vast assortment of mobile applications such as cellular phones, personal digital assistants, portable multimedia players, and digital cameras. Also, it is expected that the markets for mobile, digital consumer, and hand-held entertainment will grow steadily. These markets for mobile applications have made mobile dynamic random access memory (Mobile DRAM) as an indispensable component in the architecture of mobile systems because of its low power consumption. Generally, performance and power consumption of mobile DRAMs (LPDDRs and WIOs) depend on the configuration of system-level parameters, such as operating frequency, interface width, request size, and memory map. In mobile systems running both real-time and non-real-time applications, the memory configuration generally must satisfy bandwidth requirements of real-time applications, meet the power consumption budget, and offer the best average case execution time to the non-real-time applications [1], [2].

The increasing demand for low-power DRAM has driven JEDEC to standardize LPDDRx and WIO for mobile platforms. Significantly, JEDEC is the global leader in developing open standards for the microelectronics industry. The JEDEC's document defines the JC-42.6 in low-power memory field including the technologies of LPDDR (JESD209), LPDDR2 (JESD209-2), LPDDR3 (JESD209-3), LPDDR4 (JESD209-4), WIO (JESD229), and WIO2 (JESD229-2) [3]-[8]. In other words, JEDEC has released the first LPDDR specification in 2007 and defined the standards of LPDDR2, LPDDR3 and LPDDR4 in 2009, 2012 and 2014, respectively. On the other hand, using 3D-integration, JEDEC has also addressed this issue by standardizing WIO DRAM protocol in 2011. WIO consists of four DRAM dies vertically connected using TSV. More number of channels, wider data bus and faster interconnects make WIO DRAM a high-bandwidth memory.

The remainder of this paper is organized as follows. Section II addresses the evolutionary path and general configuration of LPDDRx memories and WIO DRAMs. The standardization definition of LPDDRx memories and WIO DRAMs from JEDEC are presented in Section III. Section IV shows the trend of mobile DRAMs. Finally, Section V concludes this paper.

II. Background

The mobile platforms generally have the issues of strict power budget and reducing memory power consumption. DRAM devices targeting mobile devices, such as LPDDR, LPDDR2, LPDDR3 and LPDDR4 memories, are already available in the market. Significantly, the LPDDR4 is expected to consume more power than previous generations because of its higher operating frequency. However, based on the issues of reducing the need of IO drivers, enabling the use of low-power CMOS transceivers, lower area requirement and higher memory bandwidth, the emerging 3D-stacked DRAM (WIO DRAM) is a promising main memory alterative for future mobile devices. The mobile DRAMs generally have evolved in a way to support higher bandwidth and power efficiency for smart devices. The evolutionary path of mobile DRAMs from JEDEC standards is illustrated in Fig. 1 [9].

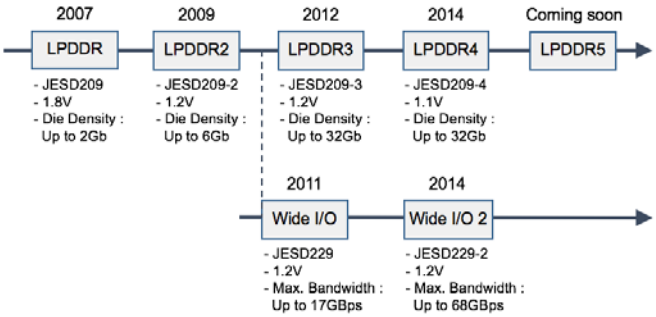

Fig. 1 The mobile DRAM evolutionary path [9]

LPDDRx memory interface is dominant in modern mobile devices. Today, almost all the mobile SoC use LPDDR2, LPDDR3 or LPDDR4. Fig. 2 shows a configuration of LPDDRx memory, which is a 1-channel, 2-rank memory subsystem with four x32 DRAM chips [10]. Generally, LPDDRx memory uses a multiplexed command/address (CA) bus to reduce the pin count. The 10-bit CA bus contains command, address, and bank information. Each LPDDRx DRAM internally has 8 banks, and each bank can process a

different memory request independently. Same as DDRx, LPDDRx accesses begin with an activation command (ACT), which includes a row access signal, a bank address, and a row address. Memory controllers send ACT commands to DRAMs, and a corresponding DRAM row is then activated (opened). After that, memory controllers issue column read or write commands with a column access signal and the starting column address for burst accesses.

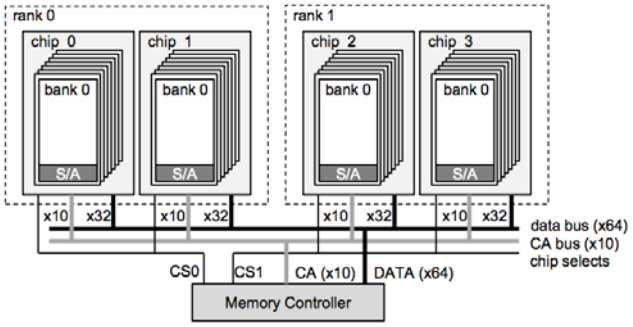

Fig. 2 The general organization of LPDDRx memory [10]

The WIO DRAM is moving from the baseline conventional DRAM architecture to 3D-stacked memories. Some biggest changes are modeled of a WIO DRAM such as, enabling 3D-stacked of DRAM dies with the help of TSV interconnects, supporting 4 independent memory-die channels, and extending I/O interfaces to 128 bits per channel. The WIO DRAM generally offers increased memory bandwidth and improved energy efficiency, due to the increased I/O interface width and reduced I/O power consumption with low capacitance TSVs connection. Fig. 3 depicts an example of the 3D-stacked WIO DRAM containing a logic die and 4 DRAM stacked dies ('ranks' in JEDEC jargon) [11]. Generally, the 4 independent memory-die channels (named a, b, c and d) illustrated in Fig. 3 including 128 bi-directional DQ data bits each and a total of 512 data bits over all 4 channels. Fig. 3 also shows each memory-die with 4 channels and the TSVs are located symmetrically in the center of the die. Significantly, the JEDEC's WIO interface allows stacking of up to 4 memory-dies on top of each other and such 4 memory-dies stacking consist of 16 channels, of which only 4 channels can be accessed at a time.

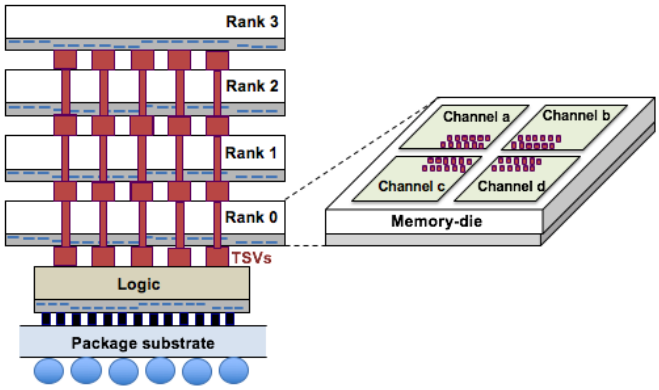

Fig. 3 3D-stacked WIO DRAM [11]

The detailed standardization definition including key features and functional description of LPDDRx memories and WIO DRAMs from JEDEC are presented in Section III.

III. Mobile DRAM Evolution

The LPDDRx memory interface is generally dominant in modern mobile devices. JEDEC released the first LPDDR specification (JESD209) in 2009. And, the revisions of JESD209B, JESD209-2F, JESD209-3C and JESD209-4A for LPDDR, LPDDR2, LPDDR3 and LPDDR4 respectively have been published in the past 5 years. On the other hand, using 3D-integration, JEDEC has addressed the issue by standardizing Wide-I/O DRAM protocol in 2011. This section will address the specifications and functionalities of the standards of LPDDRx memories and WIO DRAMs.

A. LPDDRx Series Memory

A.1 LPDDR (1)

The original low-power DDR (sometimes, in hindsight, called LPDDR1) is a slightly modified form of DDR SDRAM, with several changes to reduce overall power consumption. The standard (JESD209B) of LPDDR SDRAM was defined in Feb. 2010 [12]. This standard includes features, functionality, AC and DC characteristics, packages, and pin assignments. The purpose of this document is to define the minimum set of requirements for JEDEC compliant 64Mb through 2Gb for x16 and x32 LPDDR SDRAM devices. System designs based on the required aspects of this standard will be supported by all LPDDR SDRAM vendors providing compliant devices. Significantly, the document of JESD209 was originally numbered as JESD79-4 May 2006 to Aug. 2007 and corrected to JESD209 in Sep. 2007.

A.2 LPDDR2

A new JEDEC standard JESD209-2E defines a more dramatically revised low-power DDR interface. It is not compatible with either DDR1 or DDR2 SDRAM, but can accommodate either LPDDR2-S2: 2n pre-fetch memory (like DDR1), LPDDR2-S4: 4n pre-fetch memory (like DDR2), or LPDDR2-N: Non-volatile (NAND flash) memory. A new standard document (JESD209-2F) was published from JEDEC in June 2013 to define the LPDDR2 specifications [13]. This standard covers the technologies including LPDDR2-S2A, LPDDR2-S2B, LPDDR2-S4A, LPDDR2-S4B, LPDDR2-N-A, and LPDDR2-N-B. The purpose of this standard is to define the minimum set of requirements for JEDEC compliant 64 Mb through 8 Gb for x8, x16, and x32 SDRAM devices as well as 64 Mb through 32 Gb for x8, x16, and x32 for NVM devices.

A.3 LPDDR3

In May 2012, JEDEC published the JESD209-3 LPDDR3 standard. In comparison to LPDDR2, LPDDR3 offers a higher data rate, greater bandwidth and power efficiency, and higher memory density. LPDDR3 achieves a data rate of 1600 MT/s and utilizes key new technologies: write-leveling and command/address training, optional on-die termination (ODT), and low-I/O capacitance. LPDDR3 supports both package-on-package (PoP) and discrete packaging types. In Aug. 2015, JEDEC published the JESD209-3C LPDDR3 low-power memory device standard, targeting the performance

and memory density demands of mobile devices on high-speed 4G networks [14]. The purpose of this standard is to define the minimum set of requirements for JEDEC compliant 1 Gb through 32 Gb for x16 and x32 SDRAM devices. LPDDR3 devices use a double data rate architecture on the CA bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock. Also, LPDDR3 devices used a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 8n pre-fetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR3 SDRAM effectively consists of a single 8n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A.4 LPDDR4

In March 14, 2012, JEDEC hosted a conference to explore how future mobile device requirements will drive upcoming standards like LPDDR4. And then, in Aug 25, 2014 JEDEC published the JESD209-4 LPDDR4 low-power memory device standard. The significant changes of JESD209-4 include [15],

1. Doubling of the interface speed, and numerous consequent electrical changes, including changing the I/O standard to low-voltage swing-terminated logic (LVSTL).
2. Doubling of the internal pre-fetch size, and minimum transfer size.
3. Change from a 10-bit DDR CA bus to a 6-bit SDR bus.
4. Change from one 32-bit wide bus to two independent 16-bit wide buses.
5. Self-refresh is enabled by dedicated commands, rather than being controlled by the clock enable (CKE) line.

Also, JEDEC has published the document of JESD209-4A, LPDDR4, in Nov. 2015 [16]. The LPDDR4 is designed to significantly boost memory speed and efficiency for mobile computing devices such as smartphones, tablets, and ultra-thin notebooks. The functions of LPDDR4 will eventually operate at an I/O rate of 4266 MT/s, twice that of LPDDR3. Also, the specification of LPDDR4 is to define the minimum set of requirements for JEDEC compliant 4 Gb through 32 Gb for x16x2channel SDRAM devices. The functionalities of LPDDR4 SDRAM effectively consists of a single 16n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one half-clock-cycle data transfers at the I/O pins. Read and write accesses to the LPDDR4 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Thus, the new interface of LPDDR4 promises to have an enormous impact on the performance and capabilities of next-generation portable electronics. That is to say, LPDDR4 is intended to meet the power, bandwidth, packaging, cost and compatibility requirements of the world's most advanced mobile systems.

Generally, LPDDRx series memories use a multiplexed CA bus to reduce the pin count. And, LPDDRx accesses begin with an ACT, which includes a row access signal, a bank address, and a row address. After that, memory controllers issue column read or write commands with a column access signal and the starting column address for burst accesses. The comparisons of LPDDRx features are listed in Table 1.

Table 1 LPDDRx memory feature comparisons

Type	LPDDR (1)	LPDDR 2	LPDDR 3	LPDDR 4
Die Density	Up to 2Gb	Up to 6Gb	Up to 32 Gb	Up to 32Gb
Pre-fetch Size (Per Channel)	2n	4n	8n	16n
I/O Voltage	1.8 V	1.2 V	1.2 V	1.1 V
Max. Clock Freq.	266 MHz	533 MHz	1066 MHz	2133 MHz
Max. Data Rate (DDR)	533 MT/s	1066 MT/s	2133 MT/s	4266 MT/s
Address / Command Data Rate	SRD Rising edge of clock only	DDR Both rising & falling edges of clock	DDR Both rising & falling edges of clock	DDR Both rising & falling edges of clock

B. Wide-I/O (WIO) DRAM

B.1 WIO

The WIO mobile DRAM (JESD229), which is a breakthrough technology that will meet industry demands for increased levels of integration as well as improved performance, bandwidth, latency, power, weight and form factor, was published in Dec. 2011 by JC-42.6. WIO mobile DRAM uses chip-level 3D stacking with TSV interconnects and memory chips directly stacked upon a system-on-chip (SoC). WIO is particularly suited for applications requiring increased memory bandwidth up to 17GBps, such as 3D gaming, HD video (1080p H264 video, pico projection), simultaneously running applications, etc. WIO will provide the ultimate in performance, energy efficiency and small size for smartphones, tablets, handheld gaming consoles and other high performance mobile devices.

B.2 WIO2

WIO2 (published in Sep. 2014) offers a significant speed increase over WIO, while retaining WIO's vertically stacked TSV architecture and optimized packaging. Combined, these characteristics position WIO2 to deliver the ever-increasing speed, capacity, and power efficiency demanded by mobile devices such as smartphones, tablets and handheld gaming consoles. On the other hand, WIO2 provides four times the memory bandwidth (up to 68GBps) of the previous version of the standard, but at lower power consumption (better bandwidth/Watt) with the change to 1.1V supply voltage. From a packaging standpoint, the WIO2 die is optimized to stack on top of a SoC to minimize power consumption and footprint. The WIO2 mobile DRAM is an extension of the breakthrough technology pioneered with the publication of WIO. Just as switching to multicore processors significantly increased overall computer speed without the need to jump to a new process node, so the vertically stacked architecture allows the WIO2 interface to deliver four times the bandwidth of LPDDR4 DRAM for around one quarter of the I/O speed. It is noted that the standards of LPDDR4 and WIO2 for JEDEC offer designers a range of mobile memory solutions, allowing for maximum flexibility. Designers working with a horizontal architecture can choose LPDDR4, while those working with a vertical architecture are supported by WIO2. In either case, the committee worked to deliver the memory performance that the market requires.

Generally, WIO and WIO2 are designed specifically to stack on top of SoCs and use vertical interconnects to minimize electrical interference and die footprint. This optimizes the package's size, but also imposes certain thermal limitations, since heat radiated from the SoC has to pass through the entire memory die. The comparisons between WIO and WIO2 are listed in Table 2.

Table 2 WIO DRAM feature comparisons

Type	WIO	WIO2
Application	High end smartphones	
Interface Voltage	1.2 V	1.2 V
Interface Width	512 bits	256 bits / 512 bits
Max. Speed	Up to 266 Mbps/pin	Up to 1066 Mbps/pin
Max. Bandwidth	Up to 17 GBps	Up to 68 GBps

IV. Mobile DRAM Trend

Cadence announces the industry's first memory model for LPDDR5 in Oct. 2015 [17]. The new verification IP (VIP) product enables engineers to verify that SoC designs are compliant with the JEDEC interface standard, and that they can operate correctly in a system with the actual memory components. Validation of designs using the LPDDR5 memory model reduces the risk of mistakes, rework and delayed production, leading to faster production ramp-up and higher product quality. LPDDR5 is regarded as the next generation of low-power DRAM and is designed to speed performance, improve signal integrity and reduce refresh times. It is widely anticipated to be used in both mobile and server applications. Due to its enhanced performance, phones and tablets are expected to gain laptop-class performance, with datacenter servers maintaining performance but consuming much less energy.

Although Cadence memory model (LPDDR5) will soon come out, the related specification has not yet been published by the standard organization JEDEC. However, the JC42.6 task group (TG) kicked off the discussion of LPDDR5's specifications including, ZQ calibration, clocking and signaling, Vdd2 requirement and CA truth table at the international standard-setting meeting in Ft. Lauderdale, USA, Q4, 2015. Speculation in 2016, JEDEC will have relevant information of LPDDR5.

V. Conclusion

In the past few years, the high functionality and high convenience of mobile device products, especially the smartphone and tablet, result in the rapid growth of mobile DRAMs. Based on the keen demand of mobile DRAMs, the international standard organization, JEDEC constantly committed to the standards of mobile DRAMs to meet the industry needs and market trends. This paper addresses the evolutionary path and general structures of mobile DRAMs including LPDDRx series memories and WIO DRAMs. The standard formulation information of mobile DRAMs is also mentioned here to expose the latest trend of standards from JEDEC.

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