Low Variance Capacitor Ratio Placement for Switched-capacitor Analog Integrated Circuits

Chien-Chih Huang, Chi-Kang Chen, and Wen-Pin Hsu

***Abstract*—The key performance of many analog integrated circuits is directly related to capacitance ratios. Lower variance of capacitor ratio will result in higher yield. This study presents the placement generation of the unit capacitors with the lower variance. This study shows that the unit capacitors place as close to the central entries of the array will result in lower variance. To accomplish this, a partitioning scheme with a set of merging rules is proposed. The resultant placements achieve lower variance of capacitor ratio and thus improve the yield from 74% to 88% than the previous works.**

***Index Terms*—Capacitor Placement, Spatial Correlation Coefficient, Capacitance Ratios.**

I. Introduction

The key performance of many analog integrated circuits is directly related to capacitance ratios [1]. Due to the technology shrinking, it is anticipated that the problem of uncontrollable process variation will become more serious on parameters design [2-3]. Consider a switched-capacitor integrated circuit with the capacitor ratio C_s/C_t. Capacitance ratio mismatch problem can be alleviated by using parallel unit capacitances with the common centroid structures [4-7]. However, the layout shape must be rectangle to meet these four conditions: Coincidence, Symmetry, Dispersion, and Compactness. Moreover, which condition achieves better matching is generally difficult to determine without performing the time-consuming yield evaluation processes [8-10].

In reality, there exist some correlations among devices which highly depend on their spatial locations [11, 12]. The closer devices generally have the similar parameter variation. The study in [1] has shown that the placement with higher correlation coefficients has fewer mismatches, lower variation of capacitor ratio, and thus higher yield performance.

Consider two capacitors C_s and C_t, comprised of p and q unit capacitors, respectively, to be placed on an n-by-m array. Without loss of the generality, we assume $p \leqq q$. Conceptually, the n-by-m array is partitioned into r sub-arrays in square, $p \leqq r$. If $p=r$, then the p unit capacitors are placed on the central entries of these r sub-arrays, respectively. The placements based on the proposed partitioning scheme meet the rules of dispersion and symmetry.

On the other hand, when $p > r$, the extra $(r\text{-}p)$ sub-arrays are merged so that the total number of sub-arrays is p. Then, the p unit capacitors are placed on the central entries of these p sub-arrays. The merging rules will make the generated placement to meet the rules of coincidence and compactness.

With the proposed partitioning scheme and merging rules, the generated placements indeed meet the common-centroid rules. This study will conclude that, for the generated p sub-arrays, placing each unit capacitor on the central entry of each sub- arrays will have smaller variance than placing those on the non-central entries.

In the next section, the definitions and background are briefly reviewed. Section III presents the proposed variance-aware placement development. Finally, an experimental result on switched-capacitor circuit and brief concluding remark are given in Section IV and Section V, respectively.

II. Preliminary

The Yield is defined as the probability that the circuit under consideration meets with the design specification within the tolerance. A measure of the concentration of a random variable near its mean μ is its variance σ2. In practice, however, a circuit generally includes several design variables which are treated as random variables when taking the process variation into consideration. Thus, the variance of the random variables may affect the circuit yield.

Consider an n-by-m unit capacitor array, for any two of unit capacitors located at $\alpha=(r_1,s_1)$ and $\beta=(r_2,s_2)$, $1 \leq r_1, r_2 \leq n$ and $1 \leq s_1, s_2 \leq m$, the correlation coefficient is defined as $\rho^{D(\alpha,\beta)}$, where $0 < \rho < 1$ and the distance

$$D = \sqrt{(r_1 - r_2)^2 + (s_1 - s_2)^2}\, L \qquad (1)$$

where L depends on process and size of devices. To simplify this experiment, assume that $L = 1$ [9].

Let C_s and C_t be implemented with p and q unit capacitors, respectively, i.e., $C_s=\{C_{s1},C_{s2},\ldots,C_{sp}\}$ and $C_t=\{C_{t1},C_{t2},\ldots,C_{tq}\}$. The capacitance ratio is (p/q). The $(p+q)$ unit capacitors are placed on an n-by-m array. Let (r_i,s_i), $i=1,2,\ldots, p$, be the locations of the p unit capacitors of C_s. Minimizing $\mathrm{Var}(C_s/C_t)$ is equivalent to the minimization of ω_p [8,9],

$$\omega_p = (\frac{q}{p}+1)S_{cs} - \sum_{i=1}^{p} f(r_i,s_i) = \frac{n \times m}{p} S_{cs} - \sum_{i=1}^{p} f(r_i,s_i) \qquad (2)$$

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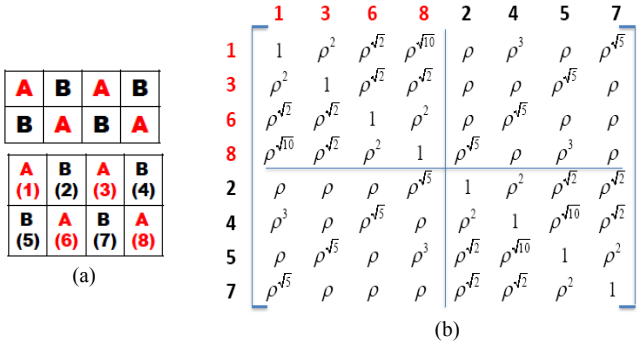
where

$$S_{cs} = \sum_{i=1}^{p-1} \sum_{j=i+1}^{p} \rho_s(i,j) \tag{3}$$

$$f(r_i,s_i) = \sum_{k=1}^{n} \sum_{j=1}^{m} \rho^{\sqrt{(r_i-k)^2+(s_i-j)^2}} \tag{4}$$

Consider the placement in Fig. 1(a), where p=q=4 on a 2-by-4 array structure. The correlation matrices are shown in Fig. 1(b). The correlation coefficient is $S_{CS}(A) = 2\rho^2 + 3\rho^{\sqrt{2}} + \rho^{\sqrt{10}}$.



(a) (b)

Fig. 1. Placement and Correlation Coefficient Matrix.

Note that $f(r_i,s_i)$ in (4) is referred to as the weight of the entry, (r_i,s_i), on the n-by-m array [8-10]. For the 8-by-8 array in Fig. 2(a), there are only 10 distinct entry weights, by (4) with ρ=0.5, the computed values are listed in Fig. 2(b), in which w1= 10.7038 is the maximum entry weight. The entries with the maximum entry weight w1 are referred to as the Central Entry/Entries (C-entry/C-entries).

w1	10.7038
w2	10.2386
w3	9.7986
w4	9.1691
w5	8.7822
w6	7.8844
w7	7.2629
w8	6.9559
w9	6.2509
w10	4.9788

Fig. 2. Computed Entry Weights.

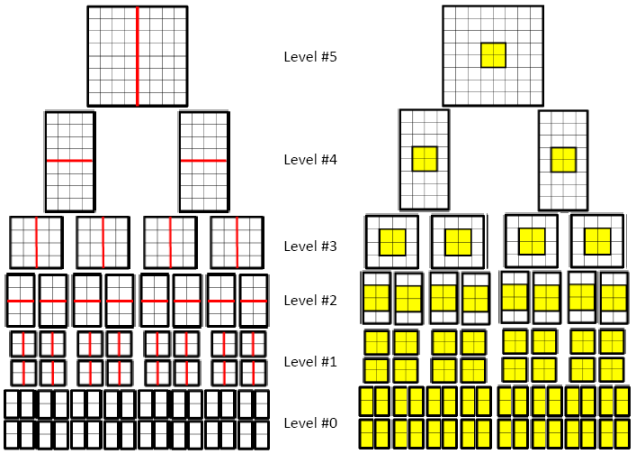
III. Variance-Aware Placement

The $(p+q)$ units of both capacitors C_s and C_t are placed on the n-by-m array. Without loss of the generality, we assume $p \le q$. If p=q=$(n\times m)/2$, then the chess-board placement is well-recognized as the least variance among the possible placements [12]. This concept leads to the development of the partitioning scheme for the variation-aware placement generation process.

A. Partition Scheme

Given the capacitor ratio C_s:C_t=p:q, $p \le q$, and the 2^R-by-2^C array, $R \le C$. The array is partitioned into r sub-arrays. In this implementation, a hierarchical partitioning scheme is presented. Basically, the 2^R-by-2^C array is partitioned into two 2^R-by-2^{C-1} sub-arrays. The partitioning process can be repeatedly applied until the size of sub-array is 2-by-1 or 1-by-2, referred to Level #0. Fig. 3(a) shows the partitioned sub-groups generated at each level, while Fig. 3(b) illustrates the C-entry/C-entries of each sub-groups, colored in yellow. In fact, given p, the partitioning process is repeatedly applied until the total number of sub-arrays, r, exceeds p, i.e., $p \le r$.

We first consider the case that r=p. Then, the p unit capacitors are placed on the C-entry/C-entries of the p sub-arrays.



(a) (b)

Fig. 3. Proposed Partitioning Scheme: (a) Sub-groups; and (b) C-entries.

Consider the p=4 and q=12 unit capacitors are placed on the 4-by-4 array in Fig. 4(a). Based on the partitioning scheme, the array is partitioned into four 2-by-2 array, the p=4 unit capacitors, colored in green, are placed on one of the C-entries, as shown in Fig. 4(a). Fig. 4(b) plots the curve family for all possible placements, where ρ is ranged from 0 to 0.99. Since each sub-array contains four C-entries in Fig. 4(a), there are 256 possible combinations of placing the unit capacitors to a C-entry of the sub-arrays. In fact, they all have lower variances and located at the cluster of the lower part of the curve families in Fig. 4(b). The curve with the lowest variance for various ρ is the placement shown in Fig. 4(a). Similarly, for the 8-by-8 array with p=4, the array is partitioned into four 4-by-4 sub-arrays, where the 4 unit capacitors are placed on one of the C-entries, colored in yellow, as shown in Fig. 4(c). Fig. 4(d) shows the 8-by-16 array is partitioned into four 4-by-8 sub-arrays, where the unit capacitor is placed on one of the C-entries in each sub-array. In fact, it has been plotted exactly the same as the curve families in Fig. 4(b), both placements in Fig. 4(c) and Fig. 4(d) achieve the lowest variances for various ρ.

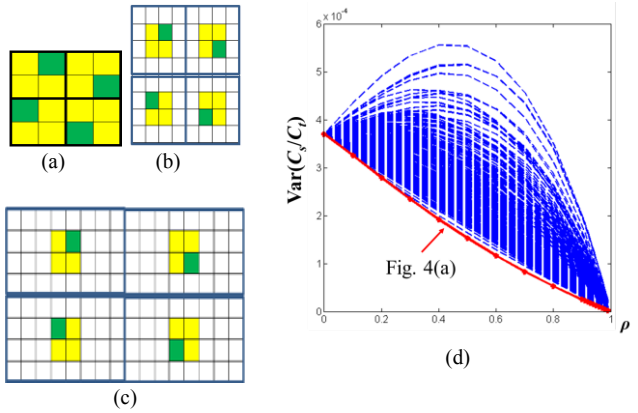


Fig. 4. Placement for p=4: (a) 4-by-4 array; (b) 8-by-8 array; (c) 8-by-16 array; and (d) Curve Families of p=4 with 4-by-4 array.

As mentioned, the array is partitioned into r sub-arrays so that $p \le r$. If p=r, then the p unit capacitors are placed on the C-entries of the sub-arrays. On the other hand, if $p < r$, i.e., more sub-arrays than requested. The next sub-section proposes a set of merging rules to make the total number of sub-arrays to be equal to p, while the generated placement still meets the common-centroid placement rules.

B. Merging Rules

This section presents the following merging rules.

Merging Rule #1:

For p= $2k$+1, the array is partitioned into 2^S sub-arrays, where $2^{S-1} \le p < 2^S$. The array is equally partitioned into upper and lower banks in each which contains 2^{S-1} sub-arrays. The placement takes k unit capacitors at the upper sub-array, while the remaining (k+1) unit capacitors are placed on the lower sub-array. Further, the 2^{S-1} sub-arrays in the upper bank are merged to k sub-arrays.

Consider p=3 (k=1) and q=13 which are placed on a 4-by-4 array (S=2). The array is partitioned into four 2-by-2 sub-arrays. By merging rule #1, we place one and two unit capacitors on the upper and lower banks, repetitively. Thus, the two 2-by-2 sub-arrays in the upper bank are merged as one 2-by-4 sub-array, as shown in Fig. 5(a). Fig. 5(b) plots all possible placements. Among them, the placement in Fig. 5(a) is the one with the least variance. Similarly, for the 8-by-8 array, the placement in Fig. 5(c) is also the one with the least variance among all possible placements.

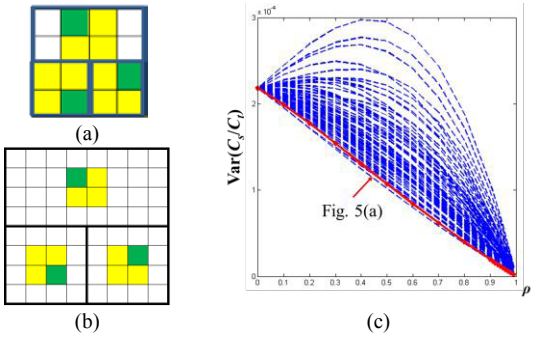


Fig. 5. Placement for p=3. (a) 4-by-4 array; (b) 8-by-8 array; (c) Curve Families of p=3 with 4-by-4 array.

Merging Rule #2:

Let r be the number of sub-arrays in a partitioned row, and t be the number of unit capacitors to be placed on these r sub-arrays, where $t \le r$. In general, by the partitioning scheme, r is even. Let r be the number of sub-arrays in a partitioned row, and t be the number of unit capacitors to be placed on these r sub-arrays, where $t \le r$. In general, by the partitioning scheme, r is even.

(a) If $t = r$, then the t unit capacitors are placed on the r sub-arrays, no merging process is needed;

(b) If $t = r - (2k + 1)$, k = 0, 1, .., r/2, then the two sub-arrays located at the center of the rows are merged, and k's two sub-arrays on its right and its left are also merged; and

(c) If $t = r - 2k$, k = 0, 1, 2, …, r/2, k's two sub-arrays on the right and left of the center points are merged.

Fig. 6 illustrates an example for Merging Rule #2, where r = 8 and t = 5~8. For t = 8, no merging process is needed. For t = 7, by (b), k = 0, the sub-arrays #4 and #5 are merged so that the number of sub-arrays is 7. For t = 6, by (c), k = 1, sub-arrays #5 and #6 on the right and sub-arrays #4 and #3 on the left are merged as shown.

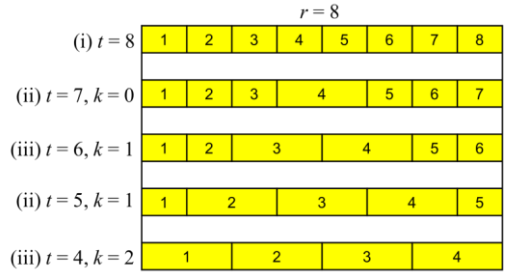


Fig. 6. Example for Merging Rule #2, where r=8, t=5~8.

Fig. 7 shows more examples to demonstrate the merging rules, where we consider the $2^3 \times 2^3$ array. The merging process can be accomplished iteratively through both merging rules (b) and (c).

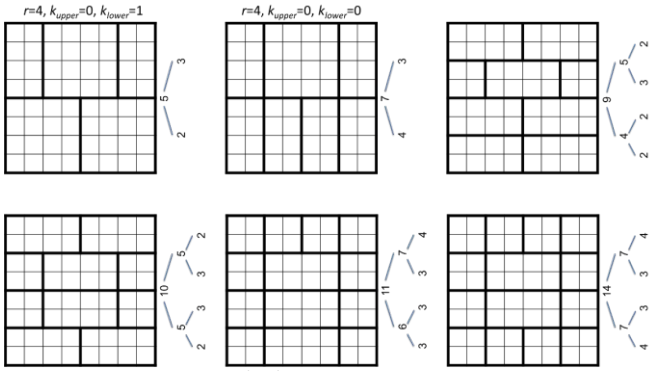


Fig. 7. Examples for $2^3 \times 2^3$ array, where p=5, 7, 9, 10, 11 and 14.

IV. Experiments

In this section, we consider the capacitor set $CS = \{C_0, C_1, C_2, C_3, C_4, C_5\}$ to the 3th-order cascaded modulator in Fig. 8. The coefficients a_1, a_2 and a_3 are derived from capacitance ratios

C_0/C_1, C_2/C_3, and C_4/C_5, respectively. Let the continued ratios $C_0 : C_1 : C_2 : C_3 : C_4 : C_5 = 8 : 40 : 3 : 10 : 2 : 5$ to be placed in a 7×10 array. Fig. 9 illustrates the placement which is generated by using the pair-sequence algorithm [11], where the dummy unit capacitor is denoted as D. Assume that the unit distance correlation coefficient ρ is 0.9, Table 1 shows the standard deviation of capacitance ratios C_0/C_1, C_2/C_3, and C_4/C_5, which are based on the placement presented in Fig. 9.

Apply the partition and merging placement schemes on the following three groups, C_0 and C_1 be placed in a 7×7 capacitor array, C_2 and C_3 be placed in a 7×2 capacitor array, and C_4 and C_5 be placed in a 7×1 capacitor array. Fig. 10(a) shows the detailed partition and merging schemes on placing $C_0 : C_1 = 8 : 40$ in the 7××7 capacitor array, $C_2 : C_3 = 3 : 10$ in the 7×2 capacitor array, and $C_4 : C_5 = 2 : 5$ in the 7×1 capacitor array, respectively. Combine the three placements in Fig. 10(a). Fig. 10(b) shows the placement for the continued ratio $C_0 : C_1 : C_2 : C_3 : C_4 : C_5 = 8 : 40 : 3 : 10 : 2 : 5$ in a 7×10 array. Similarly, assume that the unit distance correlation coefficient ρ is 0.9, the standard deviation of capacitance ratios C_0/C_1, C_2/C_3, and C_4/C_5, which are based on the placement presented in Fig. 10, are also listed in Table 1.

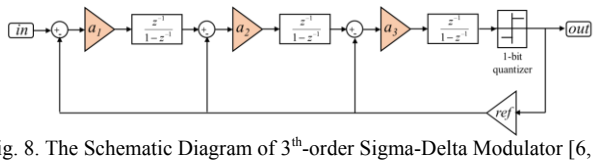
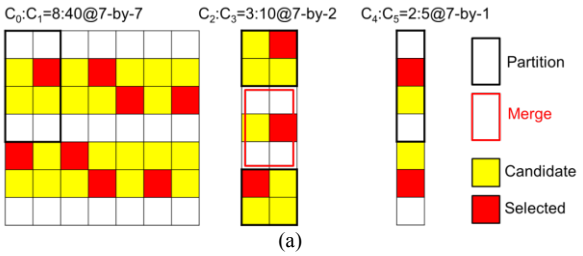


Fig. 8. The Schematic Diagram of 3th-order Sigma-Delta Modulator [6, 9].

1	1	1	1	3	0	1	1	1	D
1	1	1	3	0	5	3	1	1	1
1	3	0	2	5	4	0	1	1	1
1	1	3	D	2	5	3	1	1	1
1	1	0	4	5	2	0	3	1	1
1	1	3	5	0	3	1	1	1	1
1	1	1	0	3	1	1	1	1	1

Fig. 9. The Placement Generated by Pair-Sequence Algorithm [11].



(a)

D	1	1	1	1	1	1	3	2	5
1	0	1	0	1	1	1	3	3	4
1	1	1	1	0	1	0	3	3	5
1	1	1	1	1	1	1	3	2	5
0	1	0	1	1	1	1	3	3	5
1	1	1	0	1	0	1	2	3	4
1	1	1	1	1	1	1	3	D	5

(b)

Fig. 10. The Placement Based on Partition and Merging Schemes.

Table 1. The Evaluation of the Standard Deviation of Capacitance Ratios.

i, j	**0, 1**	**2, 3**	**4, 5**
Std(C_i/C_j) of Fig. 9.	.0058	.0093	.0093
Std(C_i/C_j) of Fig. 10.	.0025	.0060	.0106

Consider the design specification of signal-to-noise ratio (SNR) of the 3th-order SDM plotted in Fig. 8 be larger than 85 dB. Assume that the unit capacitor is 100 fF with 10% coefficient of variation (CV = 10%), the standard deviation of the unit capacitor is 10 fF, and the unit distance correlation coefficient ρ is 0.9. Apply the placement presented in Fig. 9 and Fig. 10 to the Monte-Carlo simulations [1, 6, 12], the simulation results are tabulated in Table 2, where the yield is defined as the number of "PASS" marks over the total number of samples. The total number of samples in this study are 5000. The experimental results show that the placement based on partition and merging scheme can achieve better yield performance than the placement generated by the pair-sequence algorithm.

Table 2. Monte-Carlo Simulation on Estimating Standard Deviation of Coefficients and Yield Performance.

Placement	***Std*(a_1)**	***Std*(a_2)**	***Std*(a_3)**	**Yield (>85dB)**
Fig. 9 [11]	0.0058	0.0093	0.0093	74.2 %
Fig. 10 (Proposed)	0.0025	0.0060	0.0099	87.8 %

V. Conclusion

The key performance of many analog integrated circuits is directly related to capacitance ratios. Low variance of capacitor ratio results in higher yield. This study presents a partitioning scheme and merging rules to guide the designers generating the placement with lower variance of capacitor ratio. The experimental results show that the standard deviation of first-stage coefficient and second-stage coefficient is significant reduction to 0.0025 (42% reduction) and 0.0060 (35% reduction), respectively. The proposed placement with the smaller standard deviation of coefficients improves the simulated yield from 74% to 88% than the previous works.

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